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12EC047

M.Tech. Degree Examination, June/July 2013
Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the needs for low power VLSI chips. **(06 Marks)**

b. What are the basic principles of low power VLSI design? **(06 Marks)**

c. With usual notations show that dynamic power dissipation in an inverter is given by, $P_d = C_L V^2 f$. **(08 Marks)**

2 a. Draw the energy band diagram of an unbiased MIS diode. On what factors threshold voltage (V_T) depends? Use relevant expressions. **(10 Marks)**

b. Explain inverter sizing problem and determine the optimal size of inverter chain driving a heavy load. **(10 Marks)**

3 a. Explain the advantages and limitations of SPICE power analysis method. **(05 Marks)**

b. Explain dual bit type signal model for DSP systems. How an adder (2 input – 1 output) module is characterized? **(08 Marks)**

c. Explain Monte-Carlo simulation. Derive an expression for number of samples to stop simulation. **(07 Marks)**

4 a. Derive an expression for conditional probability and frequency. **(10 Marks)**

b. Define signal entropy. Explain power estimation of combinational logic using entropy analysis. **(10 Marks)**

5 a. Explain the concept of precomputation logic with an example. **(10 Marks)**

b. Explain single driver versus distributed buffers. **(10 Marks)**

6 a. With the help of relevant diagram and equations, explain the concept bus invert encoding. **(10 Marks)**

b. Draw the circuit diagrams of, i) C^2MOS ii) TSPC iii) Non precharged TSPC and hence compare power dissipation of them. **(10 Marks)**

7 a. Discuss sources of power dissipation in DRAM and SRAM. **(10 Marks)**

b. Explain chip and package co-design of clock networks with relevant block diagrams. **(10 Marks)**

8 a. Explain power estimation, analysis and optimization techniques at algorithm/architectural level for a vector quantization design. **(10 Marks)**

b. Write short notes on: i) 8-bit Wallace multiplier.
ii) Low power bus. **(10 Marks)**

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